Chapter VIII
Design and Operation of Automatic Gain Control Loops for Receivers in Modern Communications Systems
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Introduction
This chapter will provide insight into effective operations of a Variable Gain Amplifier (VGA) in Automatic Gain Control (AGC) applications. Throughout this chapter, several key issues will be addressed.

For further discussion, an example application revolving around the AD8367 IF VGA will also be presented.

AGC Loop Design
Key Issues

- **VGA types**
- **Loop dynamics**
- **Detector types**
- **Operating level of VGA**
- **Operating level of Detector**

Figure 1 is a general block diagram for an AGC loop. The input signal passes through the VGA to produce a signal output whose level will be stabilized. The output level is measured by a detector, whose output is compared against a setpoint voltage to produce an error signal. The error signal is then integrated to produce a gain control voltage that is applied to the control input of the VGA. It may be desirable to align the maximum output level of the VGA with the maximum input level of the detector with the attenuator shown between the VGA and the detector.

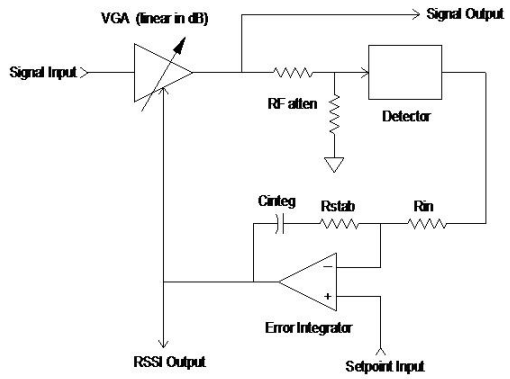


Fig. 1 VGA-Based AGC Loop Block Diagram.

VGA types:
There are two major classes of VGAs in use today. The first is the IVGA (Input VGA) that can be regarded as a passive variable attenuator followed by a fixed gain amplifier. The second type is the OVGA (Output VGA) that is equivalent to a fixed gain amplifier followed by a passive attenuator.

VGA Types

- **IVGA – Variable attenuator with fixed gain post-amplifier**
- **OVGA – Fixed gain amplifier followed by a passive attenuator**
- **IVGAs - Generally used in receivers and focus on generating a constant output level with variable input**
- **OVGAs - Generally used in transmitters to generate variable output levels with a fixed input level**
- **IVGAs - For AGC applications where constant output level is desired**

For a receive AGC system, an IVGA is the preferred choice because the available *output* level at low distortion is independent of the gain setting. Since the very object of the AGC loop is to maintain constant output in the face of a varying input signal amplitude, this is the desired trait for an AGC system.

The OVGA (whose maximum available output level decreases dramatically with decreasing gain) is ill suited to AGC applications because the undistorted output capability of the device would fall below the desired output level under some particular gain setting, thereby limiting the useful control range. OVGAs are more suited to power control applications where the objective is to vary the output level (for example, a transmitter) from a more or less constant input.

This application note is devoted to AGC systems; therefore chapter will focus on the application of IVGAs.

Analog Devices markets a wide selection of IVGAs, in which most use some variant of the

patented X-Amp architecture. In the description given above for the IVGA, the X-amp is a very close approximation in which the variable passive attenuator is a resistive ladder network with taps at equal dB intervals. Gain control is achieved by a mechanism that picks off signals from different taps as the desired gain setting is changed. Continuous variation in gain without steps or significant nonlinearity is achieved by an interpolation scheme that uses a weighted combination of signals from a few consecutive taps. As the gain is adjusted, there is a smooth handoff between tap combinations. The output from the interpolation mechanism is then passed through a low noise fixed gain amplifier. For a ladder whose taps are equally spaced in dB, this approach provides a very accurate and predictable linear-in-dB gain control with only a very small residual ripple in the gain versus the control voltage function.

Analog Devices' AD8367 is a high-performance, 45 dB input variable gain amplifier with linear-in-dB gain control for use from low frequencies up to several hundred megahertz (see Figure 2). The input is applied to a 200 Ω resistive ladder network, having nine sections each of 5 dB loss, for a total attenuation of 45 dB. At maximum gain the first tap is selected; while at progressively lower gains the tap moves smoothly and continuously toward higher attenuation values. The attenuator is followed by a 42.5 dB fixed gain feedback amplifier. The output third order intercept is +27 dBm (re 200 Ω) at 100 MHz.

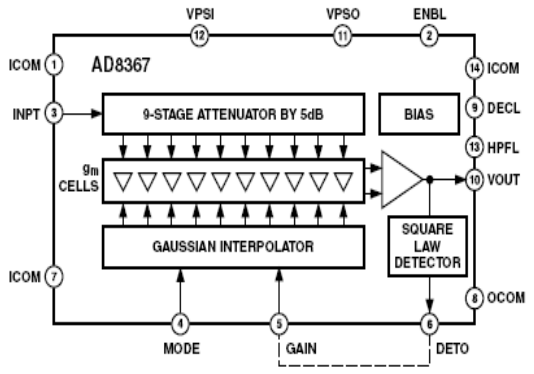


Figure 2. AD8367 500 MHz Linear-in-dB IVGA With On-Board AGC Detector

The analog gain-control interface is very simple to use. It is scaled at 20 mV/dB, and the control voltage, VGAIN, runs from 50 mV at –2.5 dB to 950 mV at +42.5 dB. In the inverse-gain mode of operation, selected by a simple pin-strap, the gain decreases from +42.5 dB at VGAIN = 50 mV to –2.5 dB at VGAIN = 950 mV. This inverse mode is needed in AGC applications that are supported by the integrated square-law detector, while the set point is chosen to level the output to 354 mV rms, regardless of the waveshape. A single external capacitor sets up the loop averaging time.

AD8367 500 MHz Linear-in-dB IVGA Key Features

- **45 dB analog variable gain range**
- **Reversible gain control sense**
- **Linear-in-dB gain control scaled 20 mV/dB**
- **On-chip square-law detector**
- **Single-supply operation: 2.7 V to 5.5 V**

When a single device is used in an AGC system, the IVGA is often criticized because the output Signal-to-Noise Ratio (SNR) may not improve with increasing input level. This is because the attenuation preceding the amplifier changes by the same amount that the signal level changes, so the input to the amplifier (which is presumed to set the noise floor) does not change, leaving the S/N unimproved.

If necessary, this behavior can be improved by cascading two VGAs and properly coordinating the gain control inputs of the two devices. If the gain control of only the second stage VGA is manipulated in the weak signal regime the signal level to the first stage VGA's amplifier *does* increase with increasing input level, so the output SNR improves. It is not necessary to begin reducing the first stage VGA's gain control input until the input level approaches the point at which the first stage would cause excessive distortion if left at full gain. At this point the gain control would be handed off to the first stage from the second stage.

Alternatively, the two gain control inputs may simply be driven in parallel, in which case the output S/N (expressed in dB) improves at half the rate at which the input level (also expressed in dB) rises. In this case each VGA is changing its gain (dB) at half the rate required to accommodate the changing input signal level. An additional benefit of this approach can be obtained if the two gain control input signals are intentionally offset by half the period of the residual ripple in the gain versus control voltage

curve. This would lead to a considerable reduction of the ripple.

Either of the above approaches to cascading VGAs leads to an increased overall gain control range, potentially twice the range of a single VGA. (For practical details of cascading VGAs, please refer to the application section of the AD603 data sheet.)

A very useful feature when using an X-amp-based IVGA in an AGC loop is the VGA's gain control voltage bears an accurate logarithmic relationship to the input signal level when the loop is in equilibrium. This means the gain control voltage may also be used as an excellent RSSI (Received Signal Strength Indicator).

Loop Dynamics:
When designing any AGC loop, response time is an important issue. There is usually a compromise that must be made between having the loop respond to undesired input level fluctuations and having it modify the legitimate amplitude modulation on the signal. Additionally, large and/or abrupt changes in the input level may lead to unwanted recovery behavior, necessitating further adjustments of the response time. Because the behavior for abrupt and/or large changes may also be strongly influenced by the detector's type, much of the discussion of this area will be deferred to the following section on detectors.

The issue of excessive loop bandwidth deserves a bit more explanation. If the loop responds too quickly, it will create undesired gain modulation arising from the loop's efforts to stabilize the output level of a signal containing legitimate amplitude modulation. This phenomenon is known as "gain pumping" and should be distinguished from the desirable gain variations made to accommodate drift and path loss variation in an AGC loop.

In the case of classic AM signals, the effect of excessive AGC bandwidth is to reduce the low frequency response of the detected audio and to introduce audio IM distortion. The AGC loop is continually adjusting the gain in an attempt to stabilize the signal amplitude; in doing so it is effectively stripping off the low frequency modulation. At the same time the gain pumping is effectively introducing fast fading, which varies the amplitude of the surviving modulation components coming out of the demodulator.

The resulting amplitude variation of some (high frequency) components in time with other (low frequency) components is the classic form of audio intermodulation distortion.

Loop Dynamics

- **AGC loop must respond to input power level changes**
- **Input level changes can be relatively slow (fading) or abrupt (pulsed applications)**
- **Excessive AGC loop bandwidth causes loop to respond to the changing envelope of input signal (gain pumping)**
- **Excessive gain pumping causes modulation errors and spectral re-growth**

In context of modern digital modulation, the presence of appreciable gain pumping can result in significant modulation errors and perhaps even noticeable spectral re-growth in extreme cases. Figure 3 shows measured gain variation over time for an AGC loop whose bandwidth was intentionally made too high for the type of signal modulation employed, in that the gain is being varied by about 1.5 dB p-p by the loop. This plot was obtained by viewing the gain control voltage of the VGA with an oscilloscope and rescaling the result to dB units. A tolerable value of gain pumping would normally be only a small fraction of 1 dB.

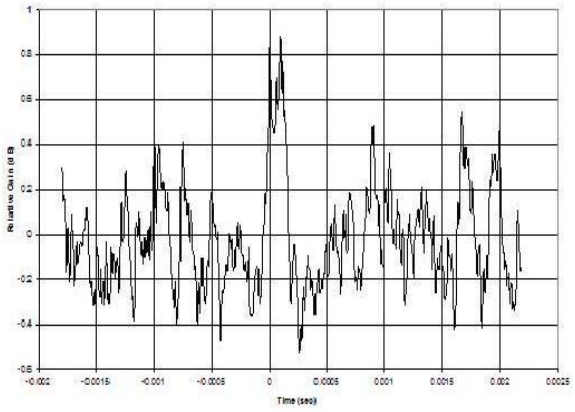


Figure 3. An AGC Loop with excessive loop bandwidth will result in gain pumping where the loop incorrectly responds to the instantaneous input power which changes on a symbol-to-symbol basis. Generally, gain pumping should be limited to a fraction of a dB.

Figure 4 shows the effect of gain pumping on a signal space constellation. This shows the demodulated constellation of a 64 QAM modulated carrier (500 kSymbols/Sec). This shows how the AGC circuit improperly responds to the varying input signal level that results from the varying levels of the symbols. In designing an AGC loop, ensure that it is fast enough to respond to average input power variations while keeping gain pumping reduced to a minimum so that it does not degrade EVM.

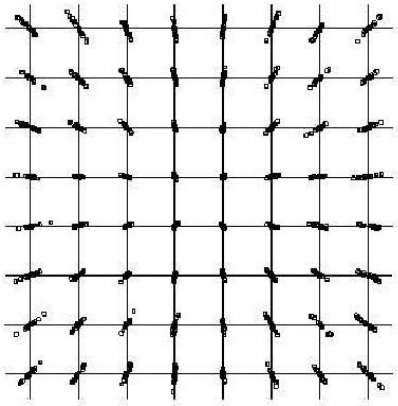


Figure 4 Excessive gain pumping in a 64 QAM Signal Space Constellation will result in degraded EVM.

Detector types
One convenient aspect of an AGC loop is that the detector does not have to have a very wide dynamic range. This is because the detector operates at a constant average level when the AGC loop is settled; thus the detector only needs to measure modulated signal levels over narrow range. However, as mentioned earlier, the detector's response law (e.g. linear, log, square law, etc) can play a significant role in determining the loop's dynamic response during large, abrupt changes in signal level. Furthermore, the choice of detector will affect the level at which the loop reaches equilibrium.

Detector Types

- **Envelope Detector**
- **Square-Law Detector**
- **True-RMS Detector**
- **Log Detector**

Envelope detector (full-wave rectifier):
The output of an envelope detector (usually a half-wave or full-wave diode circuit) is proportional to the absolute magnitude of the instantaneous RF input voltage. Assuming that sufficient low-pass filtering is applied at its output to eliminate ripple at twice the RF frequency, this detector produces a voltage proportional to the envelope amplitude of the RF signal.

Assuming that the loop's bandwidth is made small enough to avoid measurable gain pumping, the effect of the loop using an envelope detector is to stabilize the average rectified voltage of the signal. The exact result in terms of *power* is therefore dependent on the RF signal's envelope waveform. Such a loop acting on a constant-envelope signal such as FM will produce an average output power which is different than that for a heavily-amplitude-modulated signal, such as CDMA or 64 QAM, for example.

The output of the envelope detector cannot be negative no matter how weak the input signal, but even practical realizations are essentially unbounded in their response to very strong signals. The maximum detector output is likely to be determined by saturation of the VGA's output. Starting with the AGC loop in equilibrium, a sudden large increase in input amplitude causes a very large initial increase in detector output, which drives the loop rapidly towards lower gain. On the other hand, an abrupt reduction of the input signal level (regardless of how many dB) cannot reduce the detector output below zero. The loop's best response is to slew towards equilibrium at a fairly low rate until the detector output begins to change by a significant fraction of the reference voltage. At this point the recovery trends towards an exponential decay. In the slew rate limited region, the gain of the signal path is varying at a constant number of dB per second.

Envelope Detectors in AGC Loops

- **Usually a diode-based half-wave or full-wave rectifier**
- **Output power of an AGC Loop will vary with signal crest factor**
- **Fast response to fast increases in input signal to AGC Loop**
- **Slow exponential response to fast decreases in input signal**

Figure 5 shows the simulated time domain output power profile of an envelope detector based AGC loop to small input steps. (Curves for all four detector types are superimposed on this plot.) This suggests that the choice of detector has little influence on the small signal settling time of the loop.

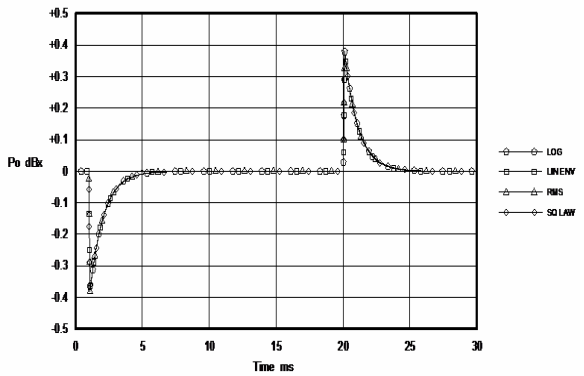


Figure 5. Simulated AGC Loop Response to Small Amplitude Steps with Log, Envelope, RMS and Square Law Detectors

Figure 6 shows the time domain output power profile of the same AGC loop to a 40 dB input step and suggests that the choice of detector has a more significant effect on settling time for large input steps. These results were obtained from simulations in which the VGA has representative limits on the gain range and on the maximum output level. The detectors contrived for these simulations have no particular limits. The theory is that in most practical situations, the designer will scale the circuit so that the detector does not limit appreciably before the VGA does.

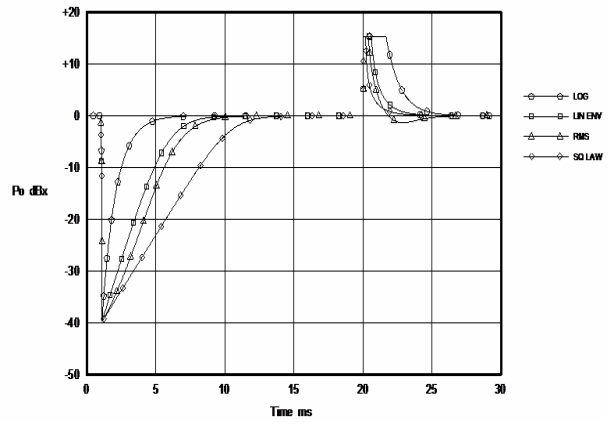


Figure 6. Simulated Response of an AGC Loop to 40 dB Input Power Steps

Square-Law Detectors

This type of detector has an instantaneous output that is proportional to the square of the instantaneous RF input voltage. This is equivalent to saying that its output is proportional to input power. This behavior, when incorporated into an AGC loop of reasonable bandwidth, makes the loop's equilibrium average output power independent of the input waveform. As with the envelope detector, the output can never go negative. This would result in the loop having a similar tendency towards slew rate limited behavior when reacting to abrupt decreases in input amplitude. The response to large abrupt increases in input amplitude can be even more striking, however, because the square-law detector response exaggerates the effect of the input increase. The extent to which this happens depends on the clipping level of either the VGA or the detector, whichever happens at a lower level.

True-RMS Detectors

This detector is a square-law detector followed by a low-pass filter followed by a square-root function. The low-pass filter performs the "mean" operation associated with the RMS (Root-Mean-Square) function, and it should have a sufficiently long time constant to smooth the output variations of the squaring detector that would otherwise arise from the legitimate modulation of the signal.

Because of the square-root element in this detector, the average output is proportional to signal voltage, not power. Therefore the loop's response to small abrupt decreases or increases of signal level should be basically the same as that for an envelope detector, provided that the added filter pole within the RMS detector is compensated correctly elsewhere in the loop. The fact that the added pole is located in a region of the signal path that is square law brings forth the possibility of the large-step response being different from that of the simple envelope detector, as seen in Figure 6. Note that the RMS detector has a slightly slower recovery from a large downward amplitude step than does the standard envelope detector, but a slightly faster recovery (and a bit of overshoot) from a step up in input amplitude.

In common with the square-law detector, the true-RMS detector will make the AGC loop's

equilibrium point independent of the RF signal waveform.

It should be noted that the presence of the long-time-constant low-pass filter in this detector may have a marked influence on loop dynamics. This filter may even provide the dominant pole in some designs. Usually the time constant must be coordinated with that of the remainder of the loop for optimum loop stability.

Square Law and RMS Detectors

- **Instantaneous output of Square Law Detector proportional to the square of the instantaneous RF input voltage**
- **Output voltage of RMS Detector is proportional to (averaged) RMS input voltage**
- **Output power of AGC Loop using RMS or Square Law Detector is independent of signal crest factor**
- **Time constant of RMS Detector must be coordinated with time constant of error amplifier in AGC Loop**

Figure 7 shows the block diagram of the ADL5500, an rms-responding power detector for use in high frequency receiver and transmitter signal chains from 100 MHz to 6 GHz. It is easy to apply, requiring only a single supply between 2.7 V and 5.5 V and a power supply decoupling capacitor. The input is internally ac-coupled with an input impedance of 50 Ω. The output is a linear-responding dc voltage with a conversion gain of 6.4 V/V rms at 900 MHz. The on-chip, 1 k Ω series resistance at the output combined with an external shunt capacitor, creates a low-pass filter response that reduces the residual ripple in the dc output voltage.

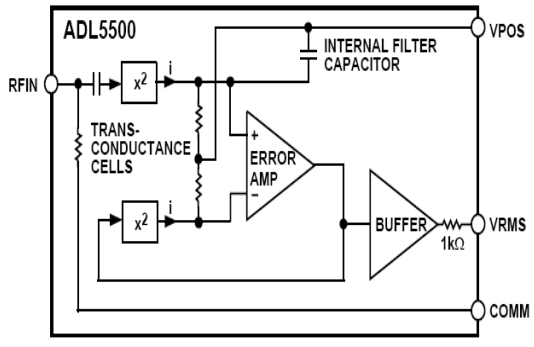


Figure 7. ADL5500 100 MHz to 6 GHz RMS Detector with Integrated Averaging Capacitor.

The ADL5500 offers excellent temperature stability with near 0 dB measurement error across temperature. The high accuracy range, centered around +3 dBm at 900 MHz, offers ±0.1 dB error from −40°C to +85°C over an 8.5 dB range. The ADL5500 reduces calibration requirements with low drift across a 30 dB range over temperature and process variations.

Log Detectors

This type of detector produces an output proportional to the logarithm of the RF input voltage. Because this behavior is complementary to that of the linear-in-dB VGA in the loop, the resulting loop dynamics are those of a linear system, assuming that signal level fluctuations during transients remain within the measurement range of the Log detector. Subject to that assumption, the AGC loop's response to abrupt and large changes in input level will not be slew-rate limited.

As with the envelope detector, the equilibrium point of an AGC loop using the Log detector will depend on the RF input waveform.

Log Detectors

- **Output proportional to the logarithm of the RF input voltage**
- **Linear-in-dB transfer function of Log Detector is complementary to gain control transfer function of Linear-in-dB X-Amp**
- **Output power of AGC Loop using Log Detector will vary with signal crest factor**

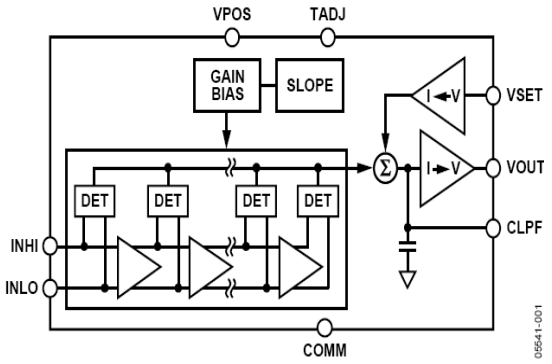


Figure 8. AD8317 1 MHz to 10 GHz, 50 dB Log Detector/Controller

The AD8317 is a demodulating logarithmic amplifier, capable of accurately converting an RF input signal to a corresponding decibel-scaled output. The device can be used in either measurement or AGC modes where it incorporates the error amplifier/integrator. The input dynamic range is typically 50 dB with error less than ±1 dB. The AD8317 has 8/10 ns response time (fall time/rise time) that enables RF burst detection to a pulse rate beyond 50 MHz. The device provides unprecedented temperature stability vs. ambient temperature conditions.

Because the output can be used for AGC applications, special attention has been given to minimize wideband noise. In this mode, the setpoint control voltage is applied to the VSET pin.

The feedback loop through an RF amplifier is closed via VOUT. The output of this regulates the amplifier's output to a magnitude corresponding to VSET. The AD8317 provides 0 V to 4.9 V output swing at the VOUT pin (on a 5 V supply), suitable for controller applications.

AD8317 1 MHz to 10 GHz Log Detector/Controller

- **50 dB detection range**
- **Built-in error amplifier for operation in AGC mode**
- **10 ns step response time**
- **Temperature stable to within ±0.5 dB**
- **AGC amplifier output swing from 0 V to 4.9 V (5 V supply)**

Comparison of responses with different detectors:
The AGC loops whose simulation results are shown in Figures 5 and 6 were designed so that the small-signal response speeds are identical. Figure 5 confirms that the AGC loop's response is independent of the detector type for small steps in amplitude. This reflects the fact that small steps traverse such a small part of the nonlinearities that slopes don't change noticeably as the response progresses.

On the other hand, Figure 6 shows that the loop's large-step transient response is markedly dependent on the type of detector. At one extreme, the Log detector gives the fastest response to large, abrupt decreases in input level because the logarithmic curve has a very steep slope for low inputs, which exaggerates the loop's response. However, the Log detector has a shallow slope for high input levels, resulting in a diminished response rate to sudden increases in signal level. At the other extreme, the square law detector's small slope, near zero input level, gives it a very sluggish response to large decreases in input amplitude. Conversely, the square law detector exaggerates the response to large signals, giving the fastest response to increasing signals. The envelope and RMS detectors, having intermediate characteristics, give response speeds in between.

Detector Comparisons When Used in AGC Loops

- **Small signal response of different detectors are similar**
- **Log detectors respond quickly to decreases in input power to AGC circuits**
- **Square Law Detectors respond quickly to increasing input signals**
- **RMS Detectors have intermediate response characteristics**

Operating Level of Detector:
Ideally the operating level of the detector should be set as high as possible in order to minimize error due to residual DC offsets. Also, the temperature stability of many detectors is best at high input power levels. However, other considerations often rule. For modulation types that involve amplitude modulation, the average input to the detector, when the loop is in equilibrium, must be lower than its maximum level. In order to form an error signal to drive the loop back towards equilibrium, even for constant-envelope signals, the settled input level must be lower than the maximum so that there is room for the detector level to increase if the system input level increases.

Setting Operating Level of Detector in AGC Loops

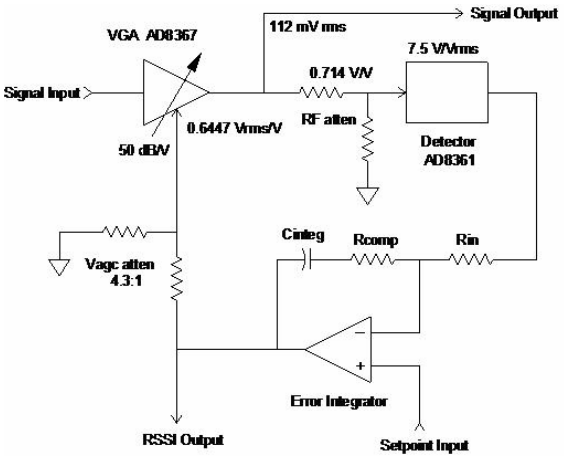
- **Set input level to detector as high as possible to minimize DC errors and temperature drift**
- **Setpoint level should be set below maximum input level to allow loop to settle in response to positive input steps**
- **Settling time for positive and negative input changes will be unequal**

Note that there will generally be unequal amounts of room for the detector output to swing up from the design equilibrium level as opposed to down, which will make the apparent attack and decay speeds of the loop differ.

Design Example of a Working AGC Loop
Now put the above considerations to work in a practical AGC loop. This design will use the AD8367 VGA. While the AD8367 VGA has an internal rms detector and AGC mode, the output setpoint level cannot be varied. As a result, in this example and external rms detector, AD8361 is used to provide a stable output. We will establish reasonable constraints for operating levels to maximize ACPR and AGC loop bandwidth, to avoid excessive gain pumping.

Design Example

- **AGC Loop constructed using AD8367 VGA and AD8361 RMS detector**
- **Modulated carrier with 18 dB peak-to-average ratio**
- **IF frequency: 380 MHz**
- **Power supply: 5 VDC**



Insert figure 9. AGC Loop Design Example

VGA output level
By doing a sweep of ACP vs. output power it can be verified that the best ACPR for the chosen frequency occurs at a VGA output level of –9 dBm, which means that the IMD3 power in the adjacent channel roughly equals the noise power in the adjacent channel. From an earlier discussion, the distortion power within the channel is about 9 dB higher than the in-channel noise. In order to achieve the best ratio of in-band signal to noise plus distortion, reduce the power to the level that brings the in-band distortion down to the noise level, which requires about 3 dB level reduction (assuming reasonably well-behaved 3rd order distortion). We therefore choose an average output level of –12 dBm from the VGA (into a total load of about 200 Ω), which is 112 mV rms.

Detector operating level
For this modulation type, the peak-to-average power ratio is about 18 dB. When operating from a 5 V supply, the maximum output level of the AD8361 is about 4.8 volts. We will presume that the squarer in the detector goes into clipping at the same input level that results in maximum output, for a CW signal (this is a slightly conservative assumption). Assuming that we don't want the peaks of our modulated signal to drive the squarer into clipping, when the loop is in equilibrium, the average output level of the detector must be at least 18 dB below 4.8 V; 4.8 * 10 ^ (-18 / 20) = 604 mV. Since the conversion gain of the detector is 7.5 V/V rms, the loop-equilibrium input level should be 604 mV / 7.5 = 80 mV rms.

This level can be obtained from the desired output level of the VGA by adding a series resistor of 90 Ω, which combines with the 225 Ω input resistance of the detector to form a voltage divider that achieves the desired result. Note that this loads the output of the VGA with 315 Ω. This means that the lowest additional parallel load impedance on the VGA would be 547 Ω in order to satisfy its design minimum load impedance of 200 Ω. In effect, more than half of the VGA's power output is going to feeding the detector, which is not very satisfying. This could be remedied by driving the VGA end of the 90 Ω resistor with an emitter follower, raising the input impedance of the overall detector by the beta of the transistor used in the follower. This would free up almost all the output drive capability of the VGA for use by the useful load.

Estimation of target AGC Loop Bandwidth
To establish the maximum loop bandwidth that will avoid intolerable gain pumping, we must make a judgment call based on an empirical measurement. In this example, we estimate that 0.5 dB p-p gain pumping is acceptable. Using a spectrum analyzer with very wide resolution bandwidth, zero span, and a linear detector, we

can estimate the desired loop bandwidth by passing a modulated signal through the spectrum analyzer to see the video bandwidth results in 0.5 dB p-p output variation. In this instance, result is 200 Hz. If necessary, this 200 Hz loop bandwidth can be re-adjusted later.

RMS Detector Filter
The RMS detector's "mean value" filter comprises an internal filter resistance combined with an external shunt capacitance. The effective value of the filter resistance varies with drive level, from about 2000 Ω at a very low drive level down to about 500 Ω at a maximum drive level. For this example we will work with a value of 1.8 KΩ.

In general, we should ascertain a suitable filter capacitance for the AD8361 rms detector by driving the circuit with a WCDMA signal. However, the previous measurement for loop bandwidth allows us to make a reasonable estimate of the required value. We found that a loop bandwidth of 200 Hz resulted in a 0.5 dB (~6%) p-p variation of detector output. This is roughly the maximum acceptable variation of RMS filter level that still gives good RMS accuracy. So, simply make the bandwidth of this filter equal to 200 Hz, which requires a filter capacitor of about 0.44 uF against the 1.8 KΩ filter resistance.

AGC Loop Design

- **AD8367 VGA delivers optimum noise and distortion at an output power of -12 dBm**
- **Set attenuation between VGA and detector to prevent clipping**
- **Set RMS detector bandwidth and AGC Loop bandwidth to 200 Hz**
- **Loop bandwidth only applies for small input deviations**

Loop Dynamics Design
We will be developing a first order loop with a small-signal bandwidth of 200 Hz. Note that the RMS detector's filter already contributes one pole at 200 Hz, so the remainder of the loop needs to take this into account. This will be achieved by choosing R_{COMP} to create a zero at 200 Hz in conjunction with C_{INTEG}. The response speed of all the other elements in the loop is so much faster than that of the desired loop that we can safely ignore all other poles.

Remember that the loop bandwidth we are designing will apply only for small deviations from the AGC loop's equilibrium level. Large transients will behave differently because of the nonlinear character of the loop.

VGA Gain
From a loop dynamics perspective, the next step is to determine the incremental gains of the VGA and of the detector. In the case of the VGA and in this context, "gain" refers the relationship between the gain control voltage and the gain of the VGA.

Use Vin and Vout to represent rms values of the VGA's RF input and output, respectively and Vg represents the gain control voltage. After reviewing the data sheet for data performance of the AD8367 for 240 MHz combined with a bit of extrapolation and rounding, it can be said that 0 dB of gain occurs at a control voltage of 0.1 V and that the control slope is exactly 50 dB/V.

First write the equation relating Vout to Vin and Vg, then differentiate Vout with respect to Vg to obtain the incremental slope needed. Notice that the slope can be expressed as a function of Vout (when the equilibrium value is known) and Vg, without direct knowledge of Vin.

(1) $GAIN = 10^{(50 * (Vg - 0.1) / 20)}$

where: 50 is the VGA control slope in dB/V, and 0.1 is the gain intercept (the control voltage giving unity gain)

(2) $V_{OUT} = V_{IN} * GAIN$

Combining (1) with (2), rearranging and multiplying yields:

(3) $V_{OUT} = V_{IN} * 10^{(-0.25)} * 10^{(2.5 * Vg)}$

Now differentiate Vout with respect to Vg to obtain the incremental slope:

(4) $dVout/dVg = Vin*10^{(-0.25)} * 10^{(2.5*Vg)} * \ln(10) * 2.5$

Next substitute (3) into (4) and evaluate $\ln(10) * 2.5$ to get:

(5) $dVout/dVg = Vout*\ln(10) * 2.5 = Vout * 5.75646$

At equilibrium, Vout is 112 mV (explained earlier); the incremental slope then evaluates to

0.112 * 5.756 = 0.6447 Vrms/V.

- $GAIN = 10^{(50 * (Vg - 0.1) / 20)}$ (1)
- $V_{OUT} = V_{IN} * GAIN$ (2)
- $V_{OUT} = V_{IN} * 10^{(-0.25)} * 10^{(2.5 * Vg)}$
- $dV_{OUT}/dVg = V_{IN} * 10^{(-0.25)} * 10^{(2.5*Vg)} * \ln(10) * 2.5$ (3)
- $dV_{OUT}/dVg = Vout * \ln(10) * 2.5 = Vout * 5.75646$ (4)
- Incremental Slope = 0.112 * 5.756 = 0.6447 Vrms/V (5)

The nominal conversion gain of the AD8361 rms detector is 7.5, from the rms value of the input to the DC output. However, remember a 90 Ω series resistor was placed at the input of the detector in order to help obtain the desired alignment of signal levels at various points in the system. This has the effect of reducing the detector's effective gain to 5.357, which is the value used in the loop analysis.

Overdrive Recovery

Recovery time from overload can be adversely affected if the output of the integrator stage is permitted to severely overdrive the gain control input of the VGA. This situation would arise if the loop is left sitting for a while with a very low (or zero) input signal level. In an effort by the loop to find more gain, the output voltage of the integrator would continue to rise until it reached saturation of the op amp. A big problem arises when a significant signal does finally arrive at the system input. Before the loop can begin reducing the gain, wait for the integrator's output to ramp back down to 1 V, which takes a while. In our circuit the maximum output voltage of the integrator is nearly 5 V, while the maximum useful control input to the AD8367 VGA is about 1.0 V. Therefore insert a resistive voltage divider of slightly less than 5:1 in the AGC path.

Calculation Of Component Values

In the loop there is a net gain (momentarily excluding the integrator) of 0.644 (VGA incremental slope) * 5.357 (effective detector slope) / 4.3 (Vagc atten) = 0.803. For a loop bandwidth of 200 Hz the loop gain should be unity at that frequency. If the rest of the loop has a gain of 0.803, the integrator must have have a gain of 1.0 / 0.803 = 1.245, which requires that the reactance of Cinteg at 200 Hz be 1.245 times the value of Rin. Mathematically, 1 / (2 Π * 200 * Cinteg) = 1.245 * Rin; Rin * Cinteg = 639.2 μs.

There is a practical constraint which is the AD8361 cannot source very much current, and can sink even less. Therefore make the value of Rin fairly high, and also provide a pulldown at the AD8361's output to improve current sinking.

Choose a rather high value of 50 kΩ for Rin in order to minimize total loading on the AD8361's output that leads to a value of 12.78 nF for Cinteg. Finally, choose the value of Rcomp to provide a loop zero at 200 Hz with Cinteg, which requires a value of 62.3 kΩ.

Circuit Tests

The exact circuit that was implemented is shown in Figure 10. The measured step response shows excellent agreement with simulation (Figure 11). Figure 12 shows the measured gain pumping, obtained by capturing the signal at the gain-control input of the VGA with an oscilloscope and scaling into dB.

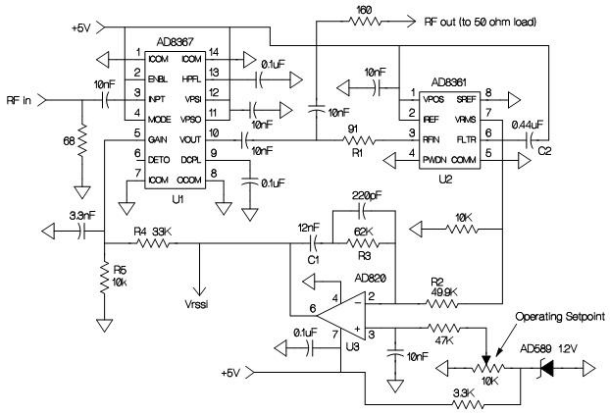


Figure 10. Complete AGC Circuit

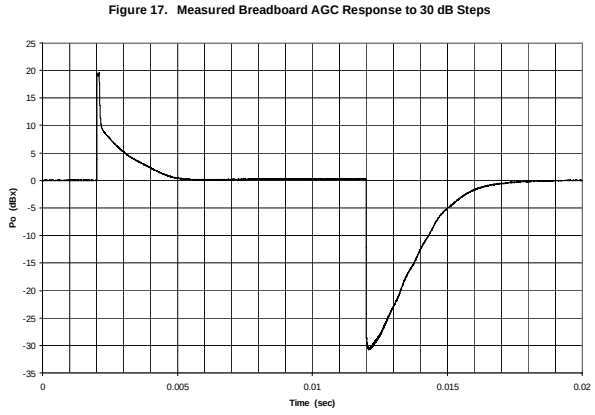


Figure 11. Measured AGC Response to 30 dB Positive and Negative Input Steps

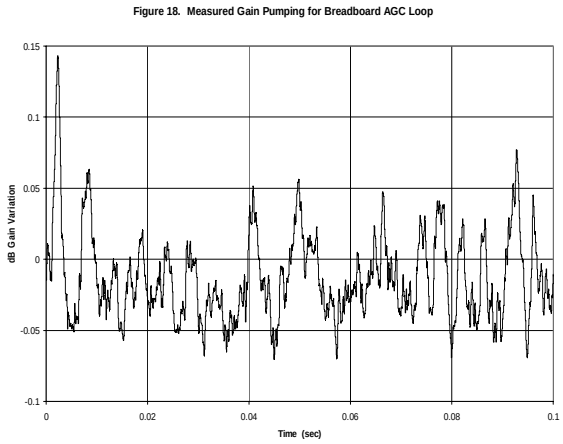


Figure 12. Gain pumping of AGC Example Circuit

Fine Tuning The Circuit

When the circuit was first tested, some unexpected overshoot (a few percent) was noted on the recovery from small amplitude steps. This was traced to an unexpectedly long detector time constant, suggesting that the rms filter capacitor had too large a value. The capacitor's value was originally calculated from an assumed value of 1.0 KΩ for the detector's internal filter resistance, which was too low. Reducing the capacitor to 0.44 uF in the circuit solved the problem.

AD8368 - A VGA With A Built-In Variable Setpoint AGC

The Analog Devices' AD8368 is a variable gain amplifier with analog linear-in-dB gain control that can be used from low frequencies to a few hundred MHz. Its excellent gain control range, conformance and flatness are attributed to Analog Devices' X-AMP ™ architecture.

The gain range of -12 to 22 dB is scaled accurately to 40 dB/V with low conformance error. The AD8368 has a 3-dB bandwidth of 800 MHz that is independent of gain setting. At 70 MHz, the OIP3 and P1dB are 33 dBm and 17 dBm, respectively. The output noise floor is –143 dBm/Hz, which corresponds to 9 dB noise figure at maximum gain. The single-ended input and output impedances are 50 Ω. The gain of the AD8368 can be configured to be an increasing or decreasing function of the gain control voltage depending on whether the MODE pin is pulled to the positive supply or to ground, respectively.

AD8368 IF VGA – Key Features

- **Analog Variable Gain Range: -12 to 22dB**
- **Linear-in-dB Scaling: 40dB/V**
- **3dB Bandwidth: 800 MHz**
- **Integrated RMS Detector and AGC Mode**
- **Output 1dB Compression: 17 dBm**
- **Output IP3: 33 dBm**
- **Noise Figure: 9 dB**
- **Input and Output Impedances: 50 Ω**

The AD8368 may be used as an AGC amplifier as shown in Figure 13. For this application, the accurate internal square-law detector is employed. The output of this detector is a current that varies in polarity depending on whether the rms value of the output is greater or less than its internally determined set point of -11 dBm. This is 178mV pk-pk for sine-wave signals, but the peak amplitude for other signals, such as Gaussian noise or those carrying complex modulation, will invariably be somewhat greater. However, for all waveforms having a reasonable crest factor (less than 13 dB), the rms value will be correctly measured and delivered at VOUT. The output setpoint may be adjusted using an external resistive divider network as depicted in Figure 13. In this configuration the RMS output voltage will be equal to (1+n)63mVrms, where n=R2/R1. For the default set-point of 63mVrms simply short R1 (direct connection from OUTP to DETI) and remove R2.

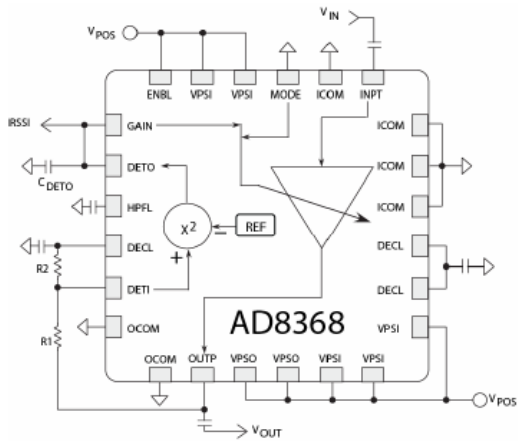


Figure 13. AD8368 IVGA with 34dB Gain Control Range with on-board AGC Detector

The AGC mode of operation requires choosing the correct gain direction. Specifically, the gain must fall as *VAGC* increases to restore the needed balance against the set-point. Therefore, the MODE pin must be pulled low. This very accurate leveling function is shown in Figure 14, where the rms output is held to within 0.2 dB of the set point for >30 dB range of input levels. This measurement was made using R1 = 100 Ω and R2 = 226 Ω to achieve 0 dBm output level.

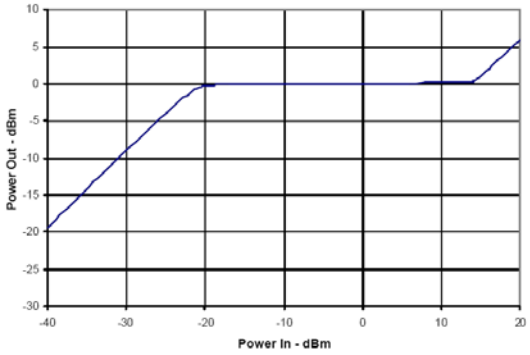


Figure 14. Output Power versus Input Power in AGC Mode at 140MHz.

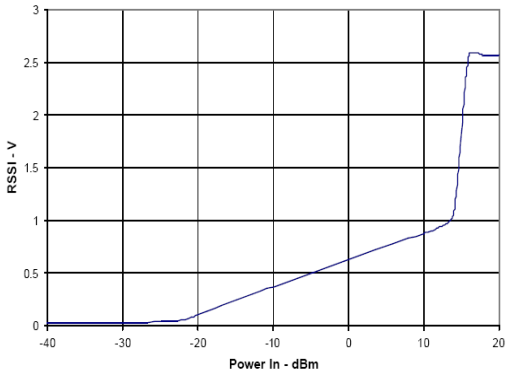


Figure 15. Monitoring the GAIN/DETO RSSI Voltage versus Input Power.

AD8368 IF VGA – AGC Mode

- **On-board AGC circuit settles to -11 dBm rms**
- **AGC setpoint can be increased using attenuator between IF output and detector input**
- **Sense of VGA gain control can be reversed to enable AGC mode**
- **AGC gain control voltage provides RMS RSSI output**

A valuable feature of using a square law detector is that the RSSI voltage is a true reflection of signal power, and may be converted to an absolute *power measurement* for any given source impedance. The AD8368 may be employed as a true-power meter by monitoring the voltage present at the DETO/GAIN interface (Figure 15).

Figure 16 illustrates the measured error-vector-magnitude (EVM) performance for a 16-QAM modulation at 10MSymbols/sec using CDETO=1000pF. At lower symbol rates the AGC loop could start to track the peak to peak transitions due to the modulation (gain pumping). At lower symbol rates it may be necessary to slow down the response of the AGC loop by increasing the value of CDETO .

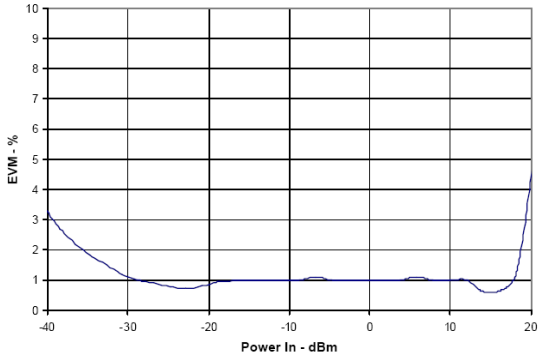


Figure 16. Error Vector Magnitude vs. Input Power for 16-QAM Carrier at 10Msymbols/sec.